In the Drawings:

Please revise the drawings in accordance with Request for Approval of Drawing Corrections attached hereto. The attached replacement sheets of drawings include changes to FIGS. 1 and 3.

Replacement sheet 1, which includes FIG. 1, replaces the original sheet 1 including FIG 1. In FIG. 1, reference number 99 has been added to illustrate a gas occupying an existing space between layer 21 (i.e., a material) and the topside 12 of semiconductor wafer 99. Additionally, reference number 98 has been added to illustrate the existing space. No new matter has been added.

Replacement sheet 3, which includes FIG. 3, replaces the original sheet 3 including FIG 3. In FIG. 3 reference number 77 has been added to illustrate a first surface of filler wafer 28 and reference number 78 has been added to illustrate a second surface of filler wafer 28. Additionally, reference number 99 has been added to illustrate a gas occupying existing spaces between the first surface 77 of filler wafer 28 and the back side 10 of semiconductor wafer 7 and the second surface 78 of filler wafer 28 and the topside 12 of semiconductor wafer 7. Reference numbers 98a and 98b have been added to illustrate the existing spaces. No new matter has been added.

REMARKS

The drawings has been amended to include reference numbers for existing gasses, spaces, and surfaces in FIGS. 1 and 3. No new matter has been added.

The specification has been amended to include descriptions of existing gasses, spaces, and surfaces in FIGS. 1 and 3. No new matter has been added.

The Examiner rejected claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21 and 22 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

The Examiner rejected claims 3 and 14 under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 1 and 12 above, and further in view of Moslehi *et al.* (5,296,385; hereinafter "Moslehi").

The Examiner rejected claims 6-9 and 17-20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 5 and 16 above, and further in view of Sugino (5,121,705).

Applicants respectfully traverse the §103 rejections with the following arguments.

35 U.S.C. §103(a)

Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21 and 22

Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21 and 22 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

Applicants respectfully contend that claims 1 and 12 as amended are not unpatentable over Koze in view of Kiyosumi, because Koze in view of Kiyosumi does not teach or suggest each and every feature of claims 1 and 12.

For example, Koze in view of Kiyosumi does not teach or suggest the feature of "wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer...forming a substructure comprising the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer, wherein a **gas** occupies **an entire space between** said **topside** of said first semiconductor wafer and said **material**" (emphasis added).

The Examiner argues: "Koze discloses a method of fabricating semiconductor wafer 100 (Fig. 1), comprising:..the first semiconductor wafer is located adjacent to the second semiconductor wafer (note in Fig. 1, any of wafers 100 could be chosen as the first and second wafers)...the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer (note Col. 1, lines 44-63, i.e., a capping layer comprising silicon dioxide and silicon nitride is formed on the backside of the wafers prior to epitaxially growing a layer on the front sides of the wafers)".

In response, Applicants respectfully contend that Koze in Col. 1, lines 44-63, does not teach or suggest forming a substructure comprising a first wafer located adjacent to a second wafer that includes a material sandwiched between a topside of the first wafer and a backside of the second wafer such that **an entire space between** the **topside** of said first semiconductor wafer and the **material** is **occupied** by a **gas** as taught by Applicant's claims 1 and 12. In contrast, Koze in Col. 1, lines 44-63 teaches "a "cap" formed on a backside of a wafer ". Additionally, Koze teaches in col. 3, lines 1-3, " Referring to FIG. 1, silicon wafers (100 are placed by pairs into wafer boats (101), so that the **active** face of one wafer **contacts** the **active** face of another ". Therefore, Applicants contend that Koze teaches an **active** face of one wafer **contacting** an **active** face on another wafer and therefore the Koze invention cannot comprise a material sandwiched between a topside (i.e., an active side) of a first wafer and a backside (a non-active side) of a second wafer such that **an entire space between** the **topside** of said first semiconductor wafer and the **material** is occupied by a gas as taught by Applicant's claims 1 and 12. Applicants define a "topside" of a wafer (i.e., in paragraph 0019) as follows: " The term " topside" of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that **comprises** or will comprise (i.e., through a wafer/semiconductor device manufacturing process) **active electrical components** (e.g., transistors, resistors, capacitors, etc.) and/or conductive wiring between active electrical components ". Additionally, Applicants define a "backside"of a wafer (i.e., in paragraph 0019) as follows: " The term "backside" of a semiconductor wafer (e.g., backside 10 of the semiconductor wafer 4 and backside 15 of the semiconductor wafer 7) is defined herein

including in the claims as a surface of a semiconductor wafer that **does not comprise active electrical components** (e.g., transistors, resistors, capacitors, etc.)".

The Examiner further alleges in response to the Office Action response filed on November 29, 2005 (i.e., in response to the Office Action mailed on September 1, 2005) that "Applicants contend that Koze does not teach or suggest forming a substructure that includes a material sandwiched between a topside of a first wafer and a backside of a second wafer, especially because Koze teaches an active face of one wafer contacting an active face on another wafer, i.e., applicants assert that Koze teaches away from claims 1 and 12. In Fig. 1 and the related text (e.g., Col. 1 beginning from line 1), Koze discloses the wafers 100 are placed by pairs into wafer boats 101, i.e., a plurality of wafer pairs are placed in each boat. Therefore, even if the active faces of two wafers are in contact with each other, one wafer of a first pair can be readily interpreted as the first semiconductor wafer in claims 1 and 12 and another wafer of a second pair would be the second semiconductor wafer of the claimed invention, wherein the front sides of each of said one wafer and said another wafer face the same direction. In other words, in Koze's disclosure, a plurality of pairs of wafers are provided in each boat such that one wafer from each of two pairs of wafers can be readily chosen to be the first and second semiconductor wafers of the claimed invention; and in choosing two wafers in such a manner, it is apparent that a substructure comprising a material (silicon dioxide and/or silicon nitride) is sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer. Therefore, applicants' remarks are not persuasive and claims 1-22 are currently rejected under 35 USC § 103 ".

In response, Applicants argue that Koze does not teach or suggest forming a substructure comprising a first wafer located adjacent to a second wafer that includes a material sandwiched between a topside of the first wafer and a backside of the second wafer such that **an entire space between** the **topside** of said first semiconductor wafer and the **material** is **occupied** by a **gas** as taught by Applicant's claims 1 and 12. The Examiner argues that " Koze teaches...In Fig. 1 and the related text (e.g., Col. 1 beginning from line 1)...wafers 100 are placed by pairs into wafer boats 101...Therefore, even if the active faces of two wafers are in contact with each other, one wafer of a first pair can be readily interpreted as the first semiconductor wafer in claims 1 and 12 and another wafer of a second pair would be the second semiconductor wafer of the claimed invention, wherein the front sides of each of said one wafer and said another wafer face the same direction...one wafer from each of two pairs of wafers can be readily chosen to be the first and second semiconductor wafers of the claimed invention; and in choosing two wafers in such a manner, it is apparent that a substructure comprising a material (silicon dioxide and/or silicon nitride) is sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the second semiconductor wafer". Applicants contend that the Examiners argument of selecting "one wafer of a first pair" and "another wafer of a second pair" of wafers "wherein the front sides of each of said one wafer and said another wafer face the same direction" in FIG. 1 of Koze (i.e., to apply to Applicants claims 1 and 12) **prevents** the "one wafer of a first pair" from being adjacent to the "another wafer of a second pair" such that **an entire space between** a **topside** the "one wafer of a first pair" and a backside of the "another wafer of a second pair " is occupied by a gas because the "one wafer " is **separated** (i.e., not next to) from the "another wafer" by a second wafer of one of the "first pair" or the "second pair (i.e., see FIG. 1 in Koze).

Therefore, Applicants contend that Koze teaches an additional wafer located between a topside the "one wafer of a first pair" and a backside of the "another wafer of a second pair thereby preventing **an entire space between** a **topside** the "one wafer of a first pair" and a **backside** of the "another wafer of a second pair " from being occupied by a gas. Therefore, Applicants contend that Koze does not teach or suggest a substructure comprising a first wafer located adjacent to a second wafer that includes a material sandwiched between a topside of the first wafer and a backside of the second wafer such that **an entire space between** the **topside** of said first semiconductor wafer and the **material** is occupied by a **gas** as taught by Applicant's claims 1 and 12. Based on the preceding arguments, Applicants respectfully maintain that claim 1 and 12 are not unpatentable over Koze in view of Kiyosumi, and that claim 1 and 12 are in condition for allowance. Since claims 2, 4, 5, 10 and 11 depend from claim 1 and claims 13, 15, 16, 21 and 22 depend from claim 12, Applicants contend that claims 2, 4, 5, 10, 11 13, 5, 16, 21 and 22 are likewise in condition for allowance.

Claims 3 and 14

Claims 3 and 14 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 1 and 12 above, and further in view of Moslehi *et al.* (5,296,385; hereinafter "Moslehi").

In response, Applicants contend that since claim 3 depends from claim 1 and claim 14 depends from claim 12 which Applicants have argued *supra* to not be unpatentable over Koze in view of Kiyosumi under 35 U.S.C. §103(a), Applicants maintain that claims 3 and 14 are likewise

not unpatentable over Koze (in view of Kiyosumi) and further in view of Moslehi under 35 U.S.C. §103(a).

Claims 6-9 and 17-20

Claims 6-9 and 17-20 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 5 and 16 above, and further in view of Sugino (5,121,705).

In response, Applicants contend that since claims 6-9 depend from claim 1 and claims 17-20 depend from claim 12 which Applicants have argued *supra* to not be unpatentable over Koze in view of Kiyosumi under 35 U.S.C. §103(a), Applicants maintain that claims 6-9 and 17-20 are likewise not unpatentable over Koze (in view of Kiyosumi) and further in view of Sugino under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

Date: 4/17/06

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